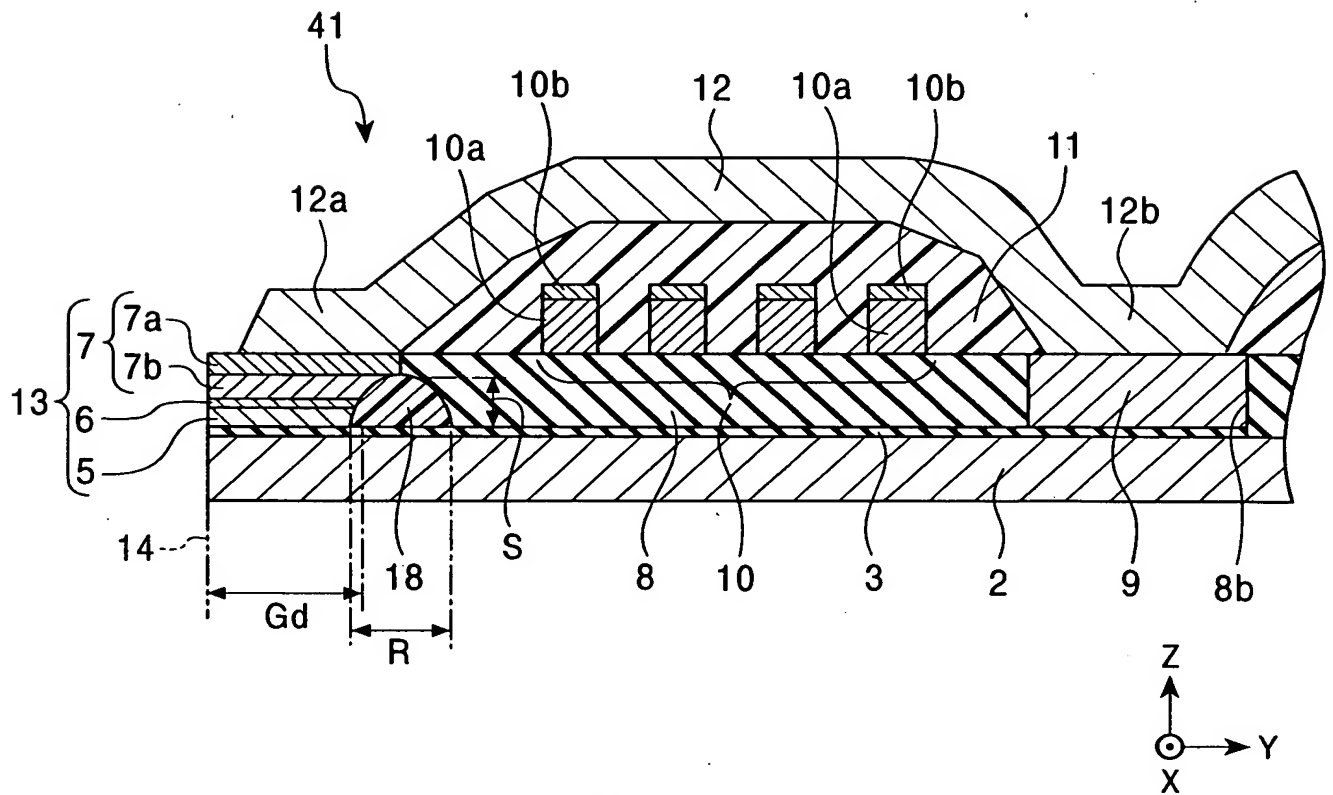


2 / 17

FIG. 3



3 / 17

FIG. 4

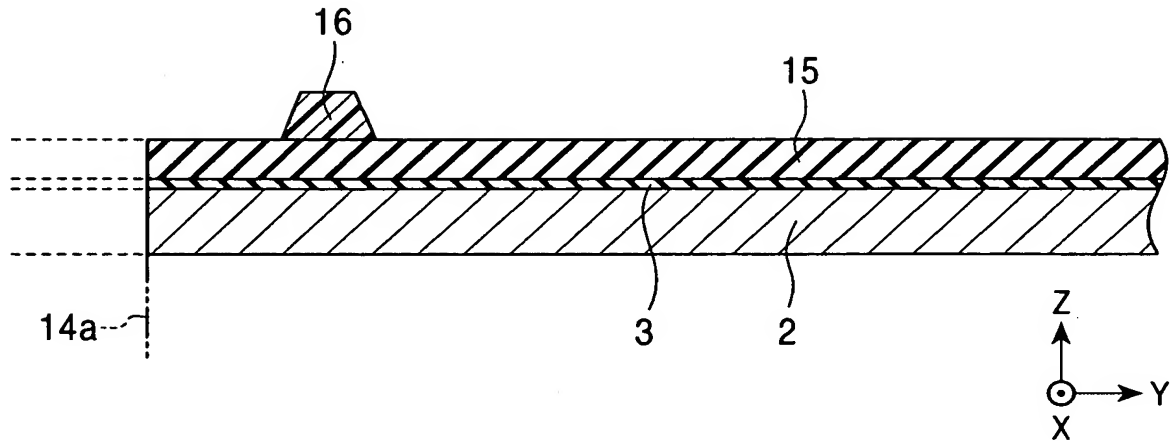


FIG. 5

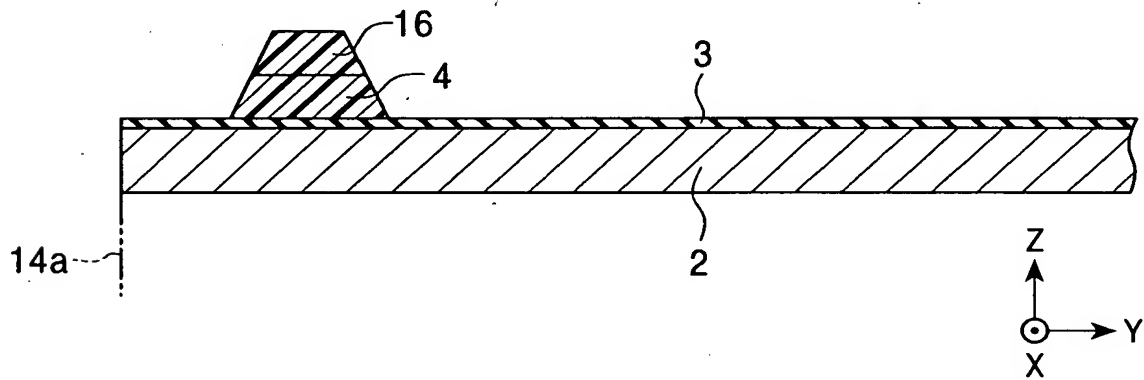
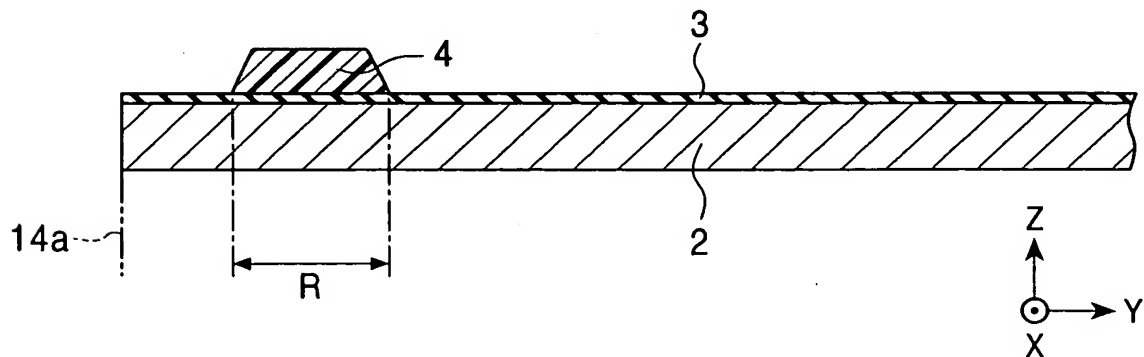


FIG. 6



10017748-121401

4 / 17

FIG. 7

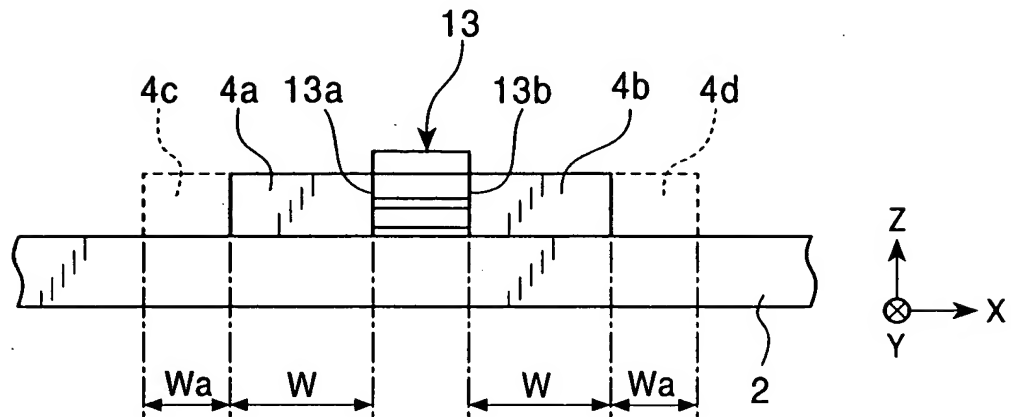
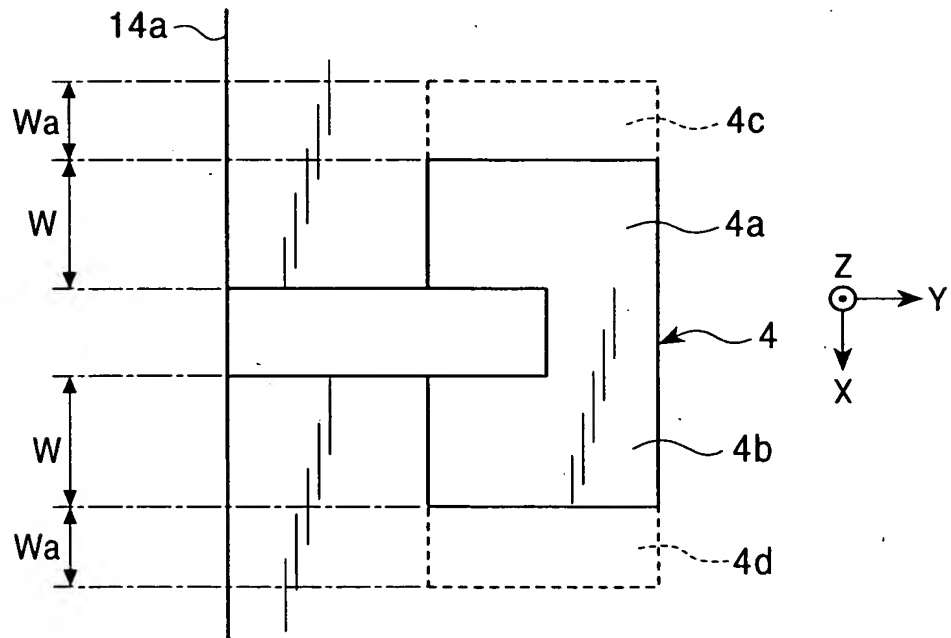


FIG. 8



5 / 17

FIG. 9

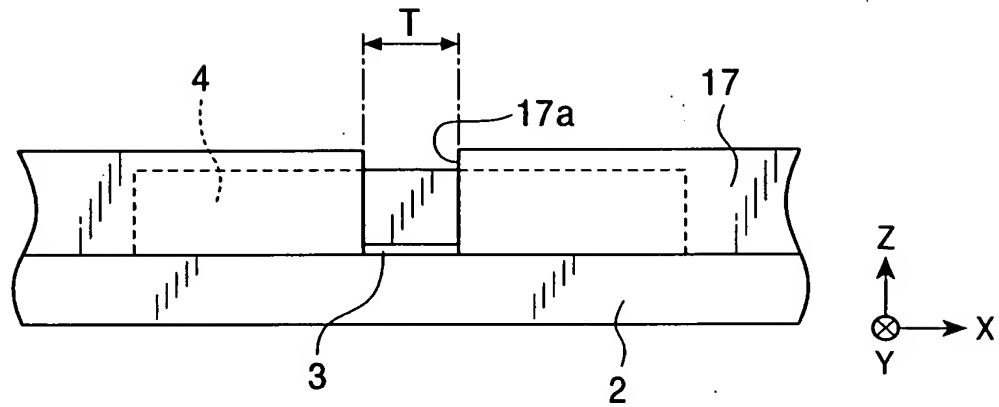
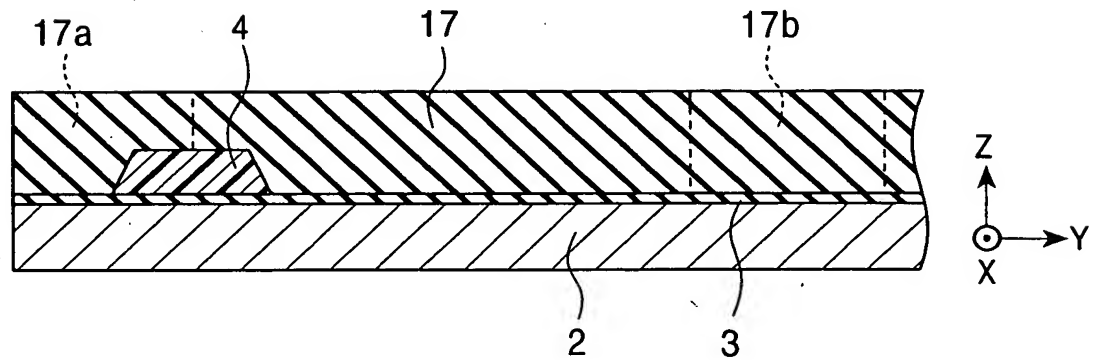


FIG. 10



6 / 17

FIG. 11

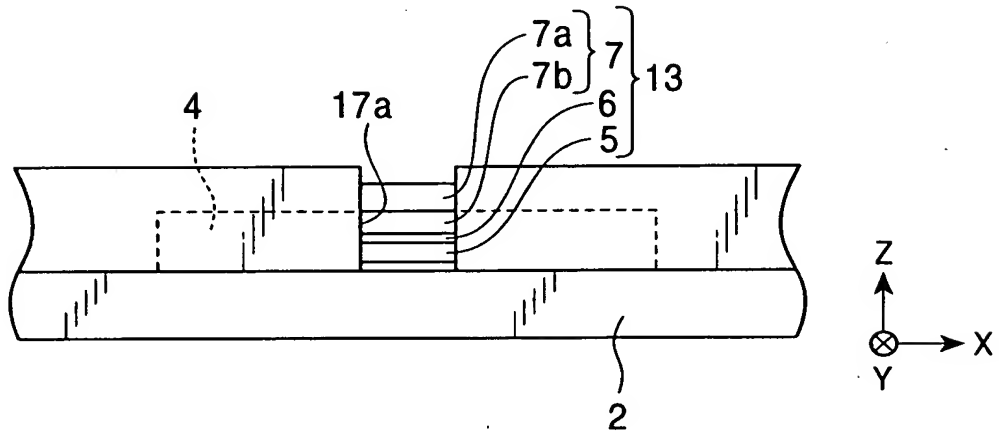
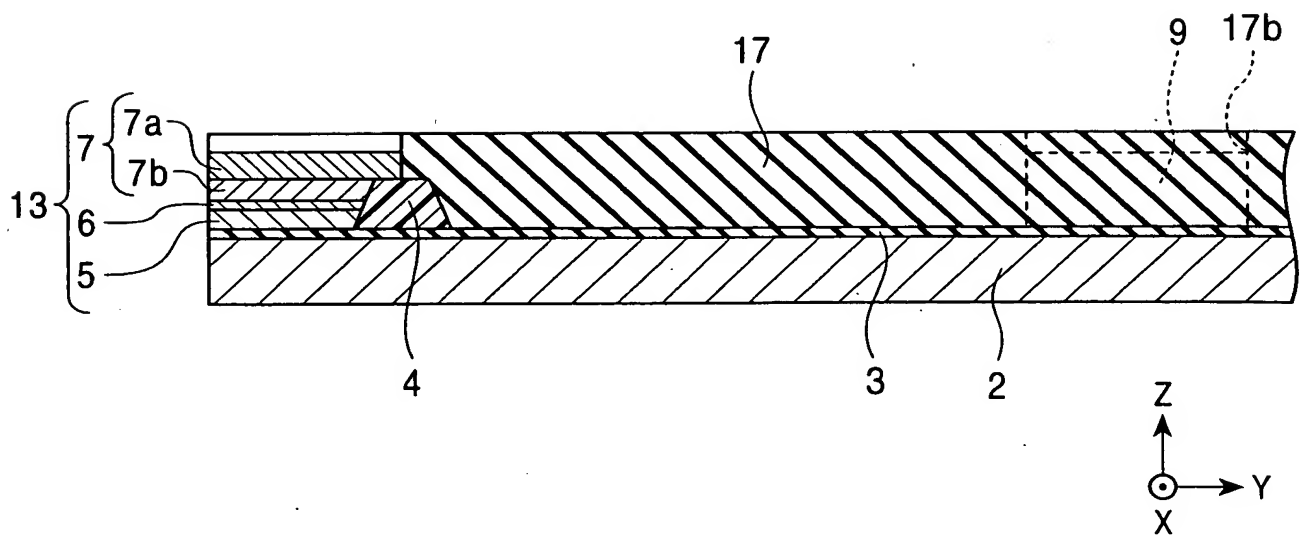


FIG. 12



7 / 17

FIG. 13

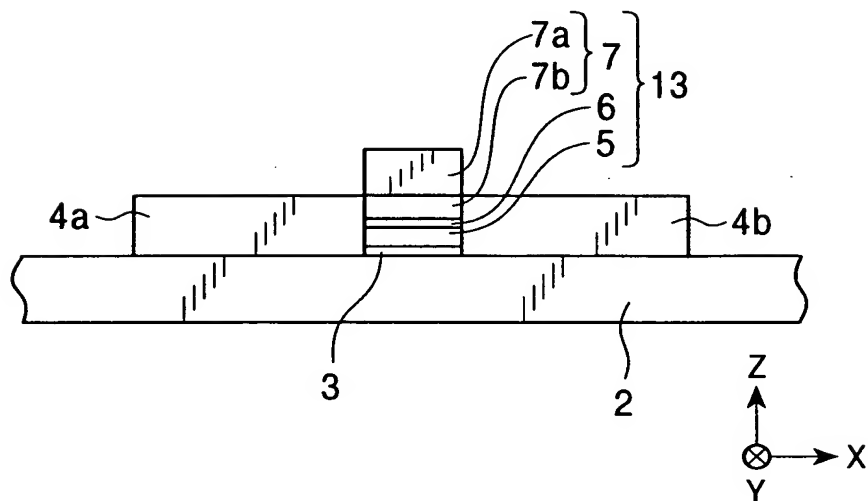
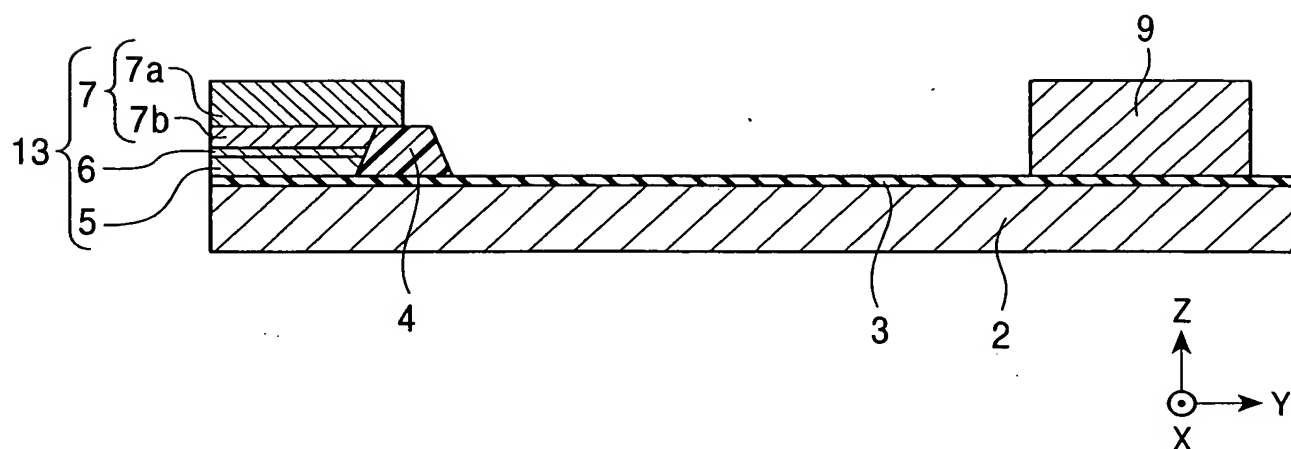


FIG. 14



8 / 17

FIG. 15

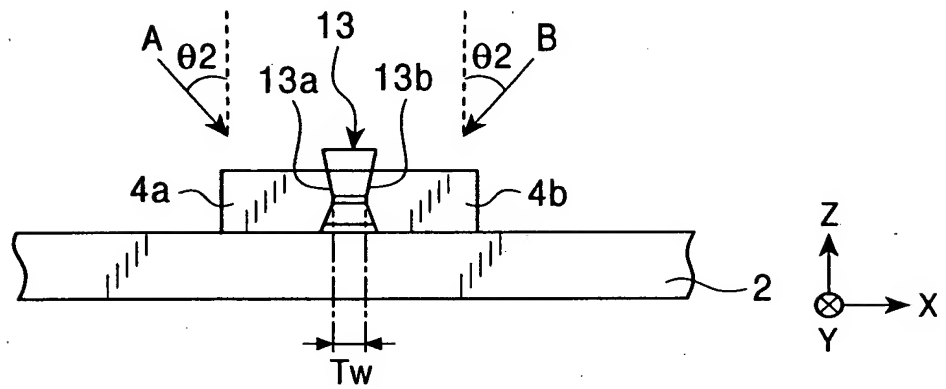
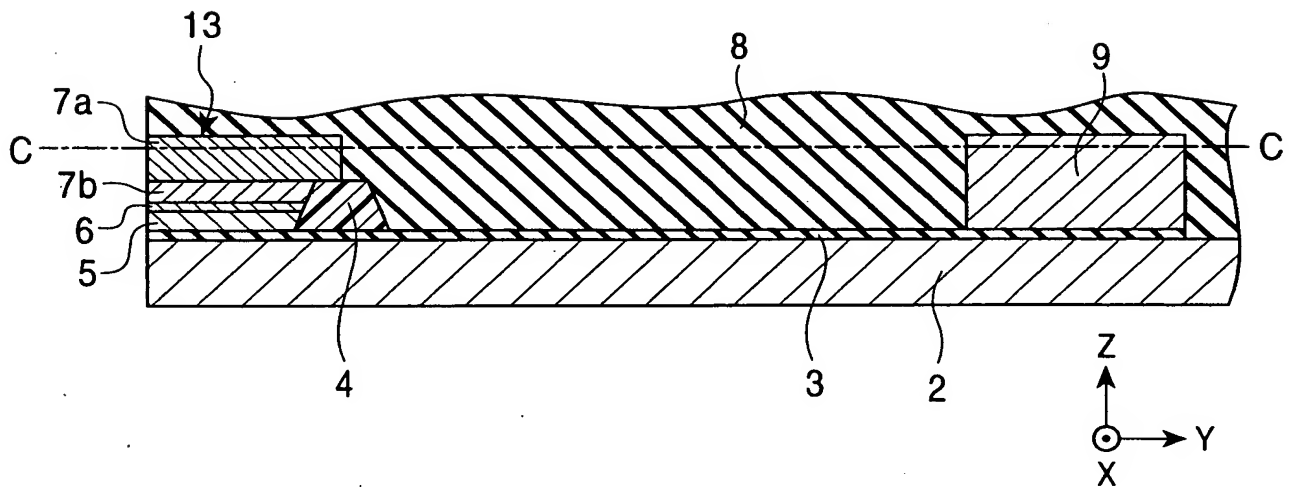
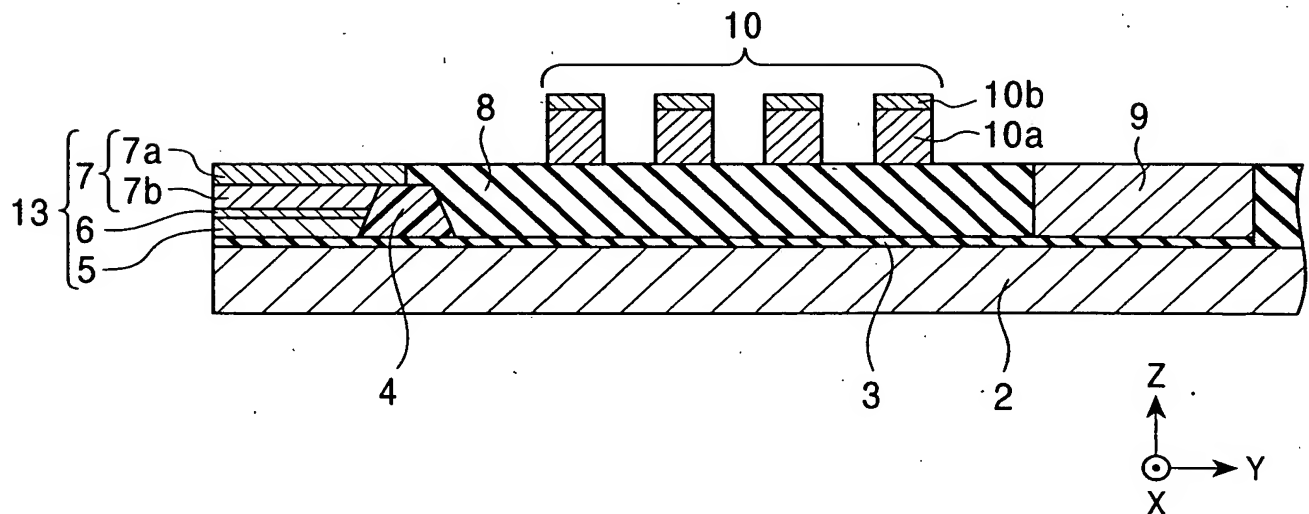


FIG. 16





10 / 17

FIG. 19

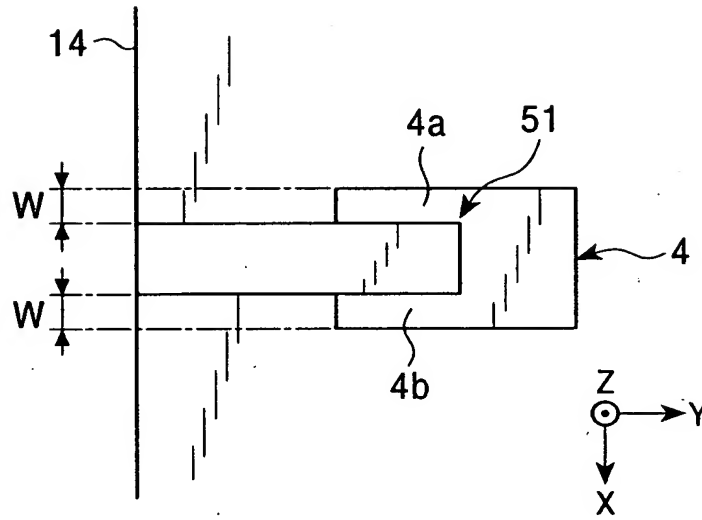
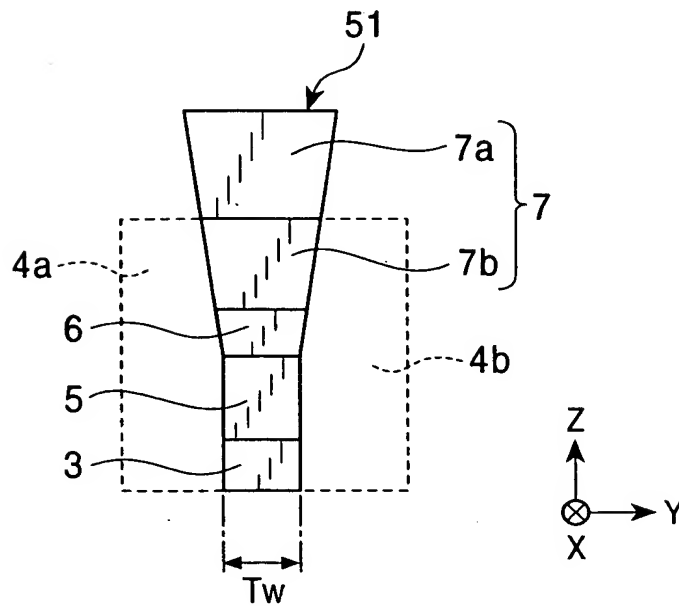


FIG. 20



11 / 17

FIG. 21

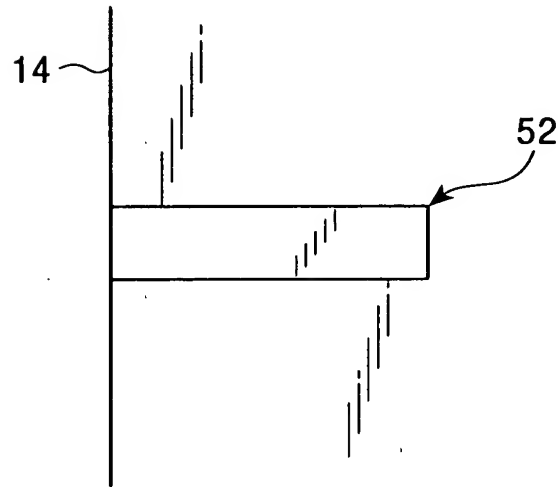
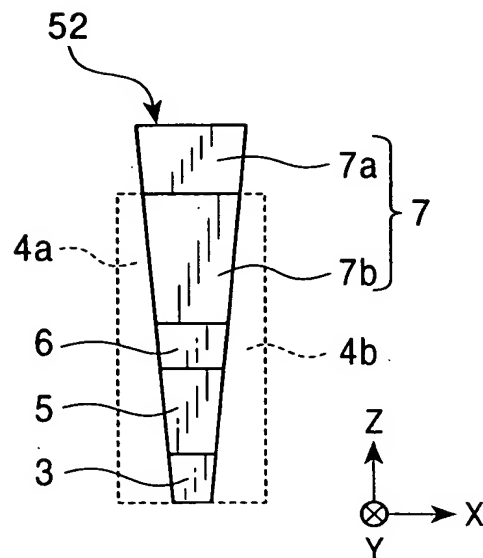


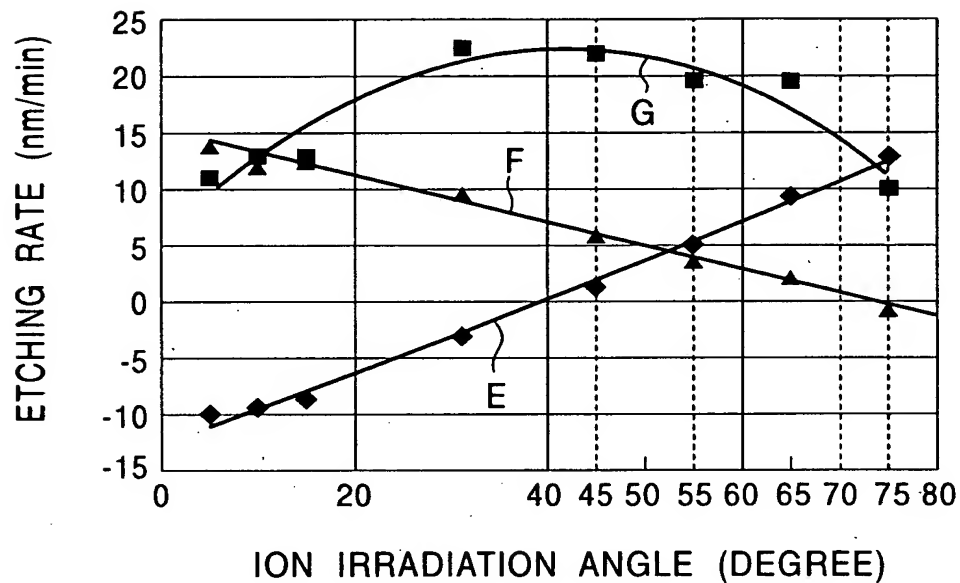
FIG. 22



10017448-11401

12 / 17

FIG. 23



- ◆ ETCHING RATE AT SIDES OF POLE SECTION
- ETCHING RATE AT UPPER SURFACE OF UPPER POLE LAYER
- ▲ ETCHING RATE AT UPPER SURFACE OF LOWER CORE LAYER AT BOTH SIDES OF POLE SECTION

A cross-sectional view of a semiconductor device. The device consists of a substrate 22 with a patterned layer 21 on top. The patterned layer 21 includes a series of rectangular blocks 30 separated by a gap Gd. The top layer 32 has a sloped side 32a and a flat side 32b. A dashed line 33 indicates a depth or distance. A coordinate system with X, Y, and Z axes is shown at the bottom right.

14 / 17

FIG. 26
PRIOR ART

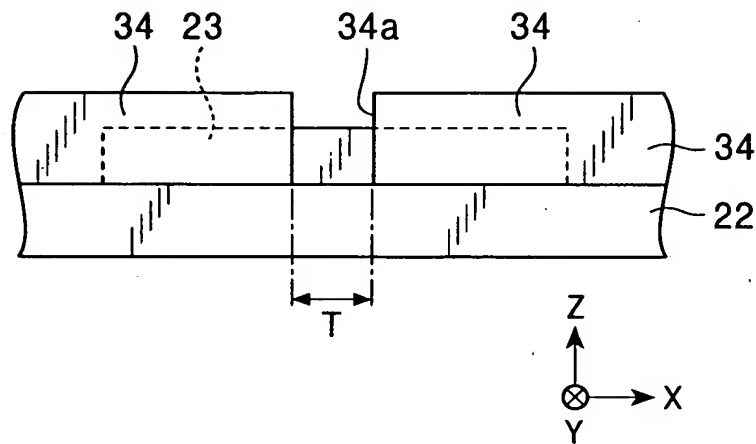
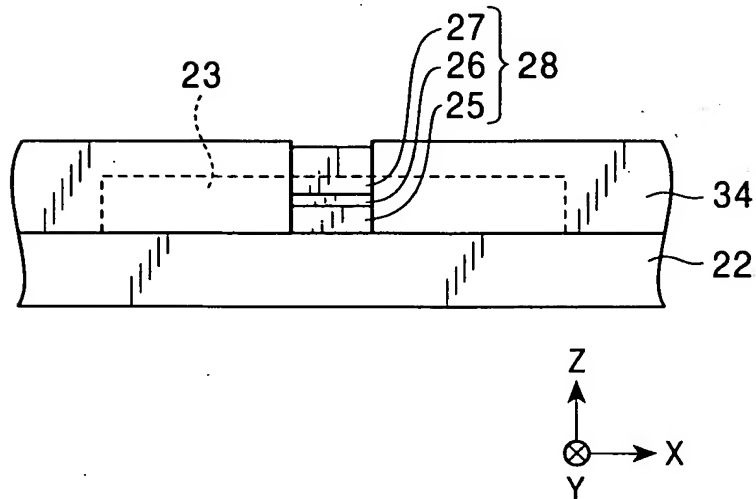


FIG. 27
PRIOR ART



15 / 17

FIG. 28
PRIOR ART

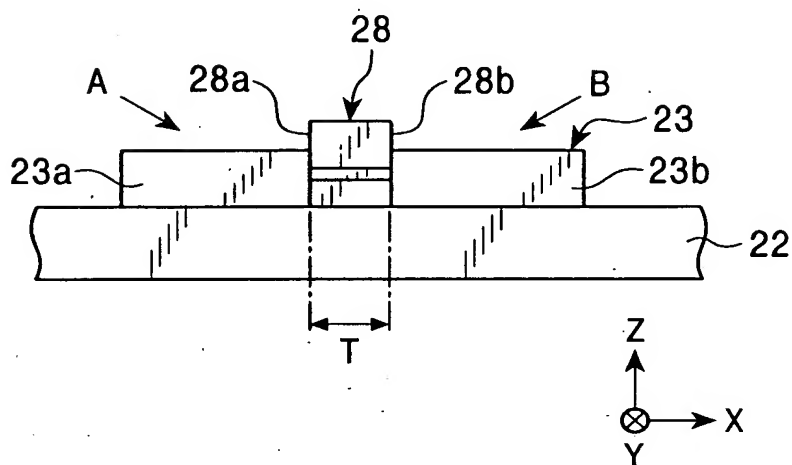
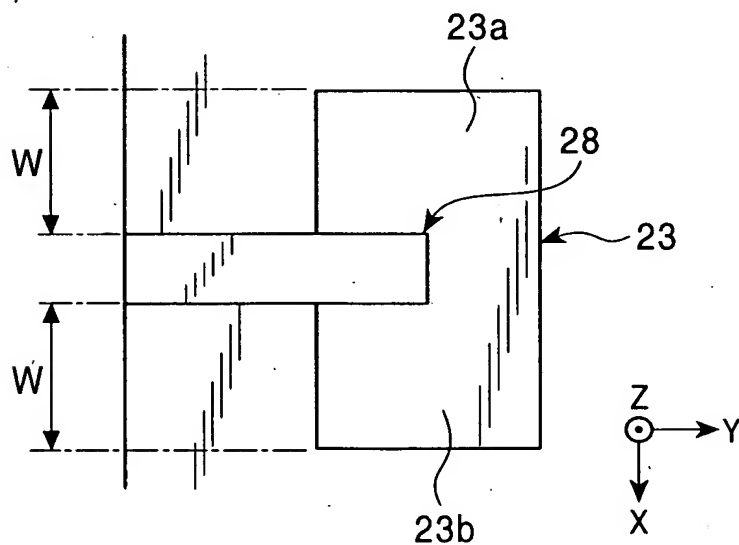


FIG. 29
PRIOR ART



16 / 17

FIG. 30
 PRIOR ART

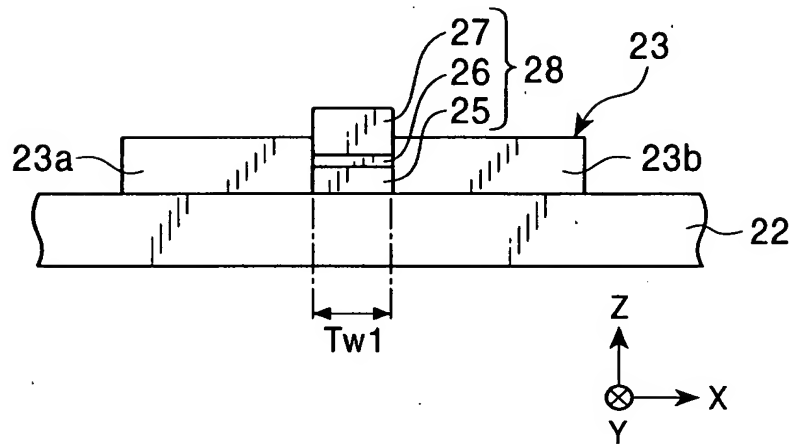
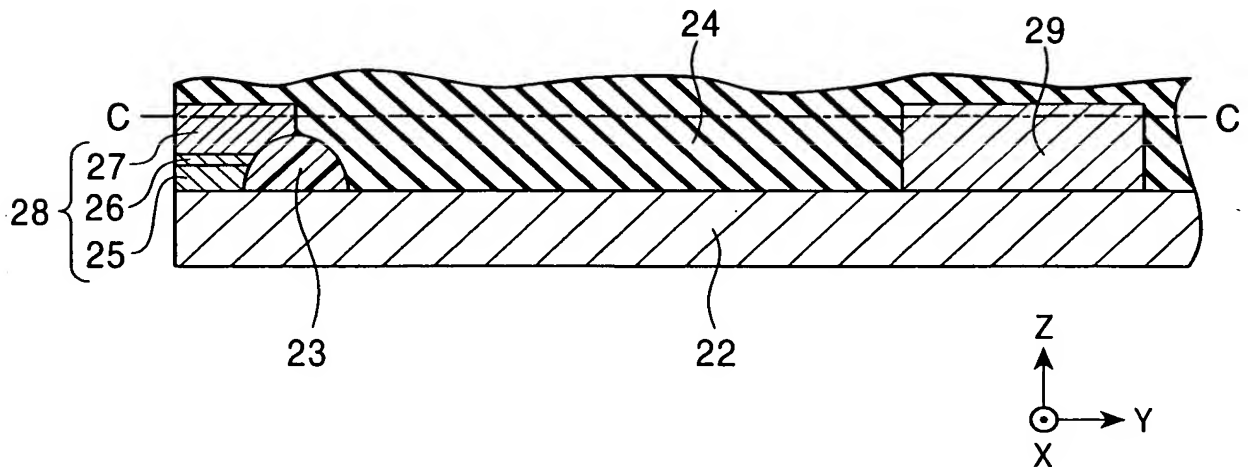


FIG. 31
 PRIOR ART



10017748-121401

17 / 17

FIG. 32
PRIOR ART

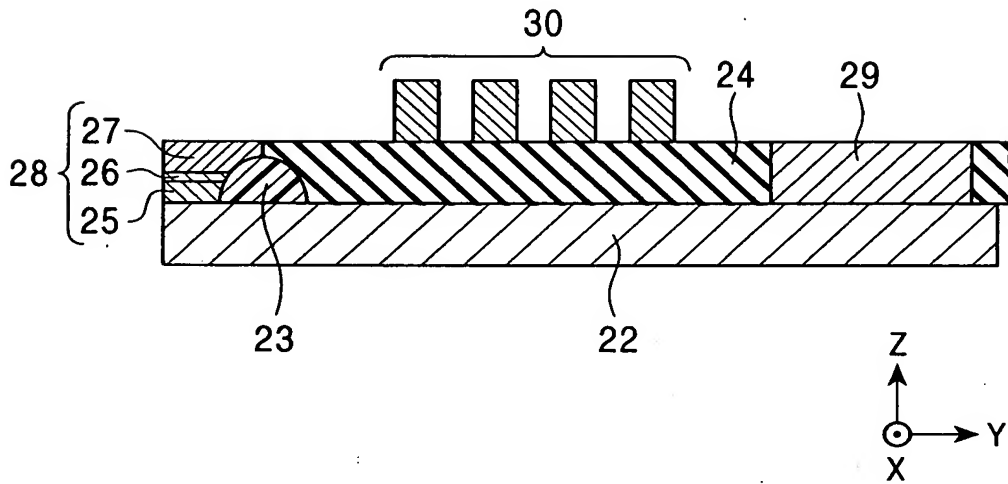


FIG. 33
PRIOR ART

